

SEP 11 2006

Atty. Dkt. No. 039153-0649 (H0982)

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1-10. (Cancelled)

11. (Currently Amended) A method of making an IC structure containing a plurality of transistors, the method comprising:

providing a first semiconductor substrate including a base layer, a strained semiconductor layer, a semiconductor/germanium layer and a first oxide layer, wherein the semiconductor/germanium layer is above the strained semiconductor layer;

attaching a second semiconductor substrate including a second oxide layer to the first oxide layer;

separating the base layer from the first substrate; and

siliciding the semiconductor/germanium layer.

12. (Previously Presented) The method of claim 28, wherein a the semiconductor/germanium layer is above the strained semiconductor layer.

13. (Original) The method of claim 12, further comprising:  
providing an aperture in the semiconductor/germanium layer.

14. (Original) The method of claim 13, further comprising:  
doping the strained semiconductor layer through the aperture.

15. (Previously Presented) The method of claim 14, wherein the doping step forms source and drain extensions.

Atty. Dkt. No. 039153-0649 (H0982)

16. (Original) The method of claim 13, further comprising:  
providing a gate conductor in the aperture.
17. (Previously Presented) The method of claim 16, further comprising:  
separating the gate conductor from the semiconductor/germanium layer with a  
spacer material.
18. (Previously Presented) The method of claim 12, further comprising:  
etching the semiconductor/germanium layer before siliciding; and  
siliciding the semiconductor/germanium layer.
19. (Original) The method of claim 11, wherein the attaching step is a hydrogen  
bonding step.
20. (Currently Amended) A method of manufacturing of an integrated circuit, the  
integrated circuit comprising a first wafer and a second wafer, the first wafer including a  
semiconductor germanium layer, a strained semiconductor layer, and a first insulating layer, the  
second wafer including a substrate and a second insulating layer, the second insulating layer  
being attached to the first insulating layer, the method comprising steps of:  
providing the first wafer including the semiconductor germanium layer, the  
strained semiconductor layer, and the first insulating layer;  
attaching the second wafer to the first wafer; and  
separating base layer from the first wafer; ~~and~~  
~~siliciding the semiconductor/germanium layer.~~
21. (Previously Presented) The method of claim 20 wherein the substrate is a bulk  
silicon substrate.
22. (Previously Presented) The method of claim 20, wherein the substrate is a  
semiconductor material.

Atty. Dkt. No. 039153-0649 (H0982)

23. (Previously Presented) The method of claim 22, wherein the semiconductor germanium layer includes a hydrogen breaking interface.

24. (Previously Presented) The method of claim 20, wherein a channel region is disposed in the strained semiconductor layer.

25. (Previously Presented) The method of claim 24, wherein a source region and a drain region are disposed in the strained semiconductor layer.

26. (Previously Presented) The method of claim 25, wherein an aperture is formed in the semiconductor germanium layer to expose the strained semiconductor layer.

27. (Previously Presented) The method of claim 26, wherein a gate structure is provided in the aperture.

28. (Currently Amended) A method of fabricating a multilayer structure containing a plurality of transistors including strained regions, the multilayer structure comprising a semiconductor/germanium layer, a strained semiconductor layer, a gate dielectric, and a gate conductor including a source and a drain provided below the semiconductor/germanium layer, the semiconductor/germanium layer having an aperture, the gate dielectric above the strained semiconductor layer and within the aperture, the gate conductor being disposed within the aperture, the method comprising:

providing a first substrate including the semiconductor/germanium layer, the strained semiconductor layer, and a first oxide layer;

attaching a second substrate including a second oxide layer to the first oxide layer; providing the aperture within the semiconductor/germanium layer; and

providing the gate dielectric and gate conductor within the aperture; and

~~providing a silicide layer above the semiconductor/germanium layer.~~

Atty. Dkt. No. 039153-0649 (H0982)

29. (Previously Presented) The method of claim 28, further comprising:  
providing a spacer in the aperture separating the semiconductor/germanium layer  
and the gate conductor.

30. (Previously Presented) The method of claim 28, further comprising:  
etching the semiconductor/germanium layer before providing a silicide layer.